



Release notes for the AArch32 Instruction Set Architecture for Arm A-profile Architecture

2025-06

Non-Confidential

Copyright © 2023–2025 Arm Limited (or its affiliates).
All rights reserved.

Issue 01

109387_2025-06_01_en



Release notes for the AArch32 Instruction Set Architecture for Arm A-profile Architecture

Copyright © 2023–2025 Arm Limited (or its affiliates). All rights reserved.

Release information

Document history

Issue	Date	Confidentiality	Change
2025_06-01	30 June 2025	Non-Confidential	2025-06 release
2025_03-01	26 March 2025	Non-Confidential	2025-03 release
2024_12-01	17 December 2024	Non-Confidential	2024-12 release
2024_09-01	30 September 2024	Non-Confidential	2023-09 release
2024_06-01	5 July 2024	Non-Confidential	2023-06 release
2024_03-01	27 March 2024	Non-Confidential	2024-03 release
2023_12-01	19 December 2023	Non-Confidential	2023-12 release
2023_09-01	29 September 2023	Non-Confidential	2023-09 release

Proprietary Notice

This document is protected by copyright and other related rights and the use or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of Arm Limited ("Arm"). No license, express or implied, by estoppel or otherwise to any intellectual property rights is granted by this document unless specifically stated.

Your access to the information in this document is conditional upon your acceptance that you will not use or permit others to use the information for the purposes of determining whether the subject matter of this document infringes any third party patents.

The content of this document is informational only. Any solutions presented herein are subject to changing conditions, information, scope, and data. This document was produced using reasonable efforts based on information available as of the date of issue of this document. The scope of information in this document may exceed that which Arm is required to provide, and such additional information is merely intended to further assist the recipient and does not

represent Arm's view of the scope of its obligations. You acknowledge and agree that you possess the necessary expertise in system security and functional safety and that you shall be solely responsible for compliance with all legal, regulatory, safety and security related requirements concerning your products, notwithstanding any information or support that may be provided by Arm herein. In addition, you are responsible for any applications which are used in conjunction with any Arm technology described in this document, and to minimize risks, adequate design and operating safeguards should be provided for by you.

This document may include technical inaccuracies or typographical errors. THIS DOCUMENT IS PROVIDED "AS IS". ARM PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT. For the avoidance of doubt, Arm makes no representation with respect to, and has undertaken no analysis to identify or understand the scope and content of, any patents, copyrights, trade secrets, trademarks, or other rights.

TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL ARM BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF ARM HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Reference by Arm to any third party's products or services within this document is not an express or implied approval or endorsement of the use thereof.

This document consists solely of commercial items. You shall be responsible for ensuring that any permitted use, duplication, or disclosure of this document complies fully with any relevant export laws and regulations to assure that this document or any portion thereof is not exported, directly or indirectly, in violation of such export laws. Use of the word "partner" in reference to Arm's customers is not intended to create or refer to any partnership relationship with any other company. Arm may make changes to this document at any time and without notice.

This document may be translated into other languages for convenience, and you agree that if there is any conflict between the English version of this document and any translation, the terms of the English version of this document shall prevail.

The validity, construction and performance of this notice shall be governed by English Law.

The Arm corporate logo and words marked with ® or ™ are registered trademarks or trademarks of Arm Limited (or its affiliates) in the US and/or elsewhere. Please follow Arm's trademark usage guidelines at <https://www.arm.com/company/policies/trademarks>. All rights reserved. Other brands and names mentioned in this document may be the trademarks of their respective owners.

Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

PRE-1121-V1.0

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by Arm and the party that Arm delivered this document to.

Unrestricted Access is an Arm internal classification.

Product Status

The information in this document is Final, that is for a developed product.

Feedback

Arm welcomes feedback on this product and its documentation. To provide feedback on the product, create a ticket on <https://support.developer.arm.com>

To provide feedback on the document, fill the following survey: <https://developer.arm.com/documentation-feedback-survey>.

Inclusive language commitment

Arm values inclusive communities. Arm recognizes that we and our industry have used language that can be offensive. Arm strives to lead the industry and create change.

We believe that this document contains no offensive language. To report offensive language in this document, email terms@arm.com.

Contents

1. AArch32 ISA Data release for A-profile Architecture (2025-06)..... 6

1. AArch32 ISA Data release for A-profile Architecture (2025-06)

30 June 2025

Product Status

The information relating to the 2024 Extensions and the rest of the A-profile Architecture is at Beta quality. Beta quality means that all major features of the specification are described, but some details might be missing.

Change History

The following changes are made to instruction descriptions:

- In VUZP (alias) and VZIP (alias), the A1 and T1 encoding condition “size == ‘10’” is added.
- In VAND (immediate) and VORN (immediate), the I16 and I32 type specifiers in the assembly syntax are corrected.
- In LSL (immediate), LSLS (immediate), and ROR (immediate), the T3 variant encoding conditions are corrected.

XML Changes

The following changes are made to the XML:

- The arch_variant tag is updated to have consistent attributes.
- The iclass id property is updated to start with the word “iclass_” appended to the iclass name.
- “[Absent]” replaces the deprecated term “(omitted)”.
- The use of the para tag is applied consistently, for single and multiple line descriptions.
- The identifiers used for ps elements are updated to be different and unique.
- Docvars are produced for an alias as defined by its parent.
- Symbol links are updated to match architectural meaning.
- Hover text is updated to match the description.
- The references in descriptive text are updated to use the register_link tag.
- encodedin entries are populated more accurately.
- The assembler syntax prototype is updated to show two or more consecutive spaces.
- Symbols that appear only in the parent no longer appear in the “Assembler Symbols” section of the alias.
- The order of the symbol descriptions is updated to follow the order of the instructions.
- Parentheses around symbol choices appear consistently.
- Hex values are updated to present consistently in upper case.
- The operational information for an alias or pseudo-instruction is specified only in its parent.

- Alias conditions are updated to follow the order of the instructions.
- Most Arm-defined words are updated to have the correct tags.
- Optional symbols links are updated to not include curly brackets in the link.
- In the assembler description, UInt presentation is updated to be consistent.
- Rendering is updated to show separation bars only between fields at an instruction's own level. Fields that are defined in the current instruction diagram appear.
- Spacing between optional symbols and commas are updated to be consistent.
- In the index by encoding, UNALLOCATED entries are listed more consistently.
- Instructions that have an alias that has more than one variant list all those variants.
- Operand docvars are not used.
- The contents of encoding name label are removed if they repeat information.
- Tags used within desc are brief and authored, and para is used consistently within brief.
- para tags are used within some listitem entries.

Many simple clarifications and corrections are also present, but are too small to be listed here. Some minor formatting changes are suppressed and not highlighted in the diff output.

Known Issues

All issues identified in the below list will be fixed in a future release.

- There is a mismatch between the encoding for VMOVL and some other instructions and the conditions defined for the groups they appear in. The encoding is correct. The group conditions for affected instructions will be clarified.
- The setting of FPEXC.DEX and FPEXC.TFV bits for an invalid FPSCR.Len and FPSCR.Stride, for an allocated CP10 or CP11 instruction will be added to the pseudocode.
- In the T32 encoding index, the condition “op0<1n> == 1” will be restored to the “Load/store dual, load/store exclusive, load-acquire/store-release, and table branch” group.
- In the A32 encoding index, field names that are referred to in “The following constraints ...” text but are not included in the relevant encoding diagrams will be added to the relevant encoding diagrams.
- In the XML, some cases of **UNKNOWN** are not encased in arm-defined-word tags.

Potential Upcoming Changes

The details of the architecture are presented in pseudocode in Architecture Specification Language (ASL). Arm is defining a new version of the Architecture Specification Language, ASL1, to improve and expand the capabilities of the language. Please see <https://developer.arm.com/Architectures/Architecture%20Specification%20Language> for details on this language. Arm will be publishing an equivalent release in ASL1 format later in 2025.

Intention and quality statements for all ArmARM architecture releases

The intention and scope of the Architecture releases is to describe changes from the existing architecture to the next release. The quality of the architecture releases refers to the accuracy and completeness of the changes described in the specifications.

The intention and scope of the AARCHMRS and Data releases is to describe the content and behavior of the registers, system registers, instructions, pseudocode and features of the architecture in full, for human readers in a way that enables correct information for the current or any previous release can be deduced. The quality of the XML releases refers to the accuracy and completeness of the content to a human reader.

The intention and scope of the JSON releases is to describe aspects of the AARCHMRS and Data releases in a structured, machine readable format. The content of the AARCHMRS and Data architectural content will be approximately equivalent to the corresponding XML release. However there are some aspects of the architecture which cannot yet be represented in a machine readable format. The content of the AARCHMRS architectural content will be approximately equivalent to the corresponding Data release.

The intention and scope of the Schema for the JSON releases is to describe the syntax and format of the json files used in the json releases. The schema is still under development and is subject to change.